CLAIMS

What is claimed is:

1. A method of operating a signal processing device, the method comprising:

receiving a signal sample;

encoding the signal sample using a coding process to produce symbolic values;

modifying the symbolic values to reduce a number of digits used to represent the symbolic values and produce coded values; and

processing the coded values in the signal processing device.

2. The method according to claim 1, wherein the coding process is a radix 4 Booth coding process.

3. The method according to claim 1, wherein modifying the symbolic values comprises changing at least one value of a digit in the coding process based upon a value in a next higher order digit of the symbolic value to create a coded value.

4. The method according to claim 1, wherein processing comprises using the coded values as input to the signal processing device, and the signal processing device comprises a digital filter.

5. The method according to claim 4, where the digital filter comprises a finite impulse response filter.

6. The method according to claim 1, wherein processing the coded values in the signal processing device further comprises:

inputting the coded values to the signal processing device;

multiplying the coded values by coefficients forming a plurality of products;

summing the products to produce a processed signal;

delaying output of the processed signal by at least one unit delay; and

outputting the processed signal.

7. The method according to claim 6, wherein multiplying the coded values by coefficients forming a plurality of products further comprises:

directing the coded values to a plurality of multipliers and a plurality of sign inverters;

multiplying the coded values by first coefficients in the multipliers to form at least one first product; and

multiplying the coded values by at least one second coefficient in the sign inverters to form at least one second product.

8. A method of increasing a bit rate of transmission of a signal, the method comprising:

receiving a signal sample;

encoding the signal sample using a coding process to produce symbolic values having a particular number of digits;

modifying the symbolic values to reduce the number of digits used to represent the symbolic values and produce coded values; and

processing the coded values in a signal processing device.

9. The method according to claim 8, wherein reducing the number of digits used to represent symbolic values further comprises:

eliminating at least one digit during the coding process without losing any digital information; and

processing more digital information per unit time with fewer processing operations.

10. The method according to claim 8, wherein the coding process is a radix 4 Booth coding process.

11. The method according to claim 8, wherein modifying the symbolic values comprises changing at least one value of a digit in the coding process based upon a value in a next higher order digit of a symbolic value to create a coded value.

12. The method according to claim 8, wherein processing comprises using the coded values as input to the signal processing device, and the signal processing device comprises a digital filter.

13. The method according to claim 12, where the digital filter comprises a finite impulse response filter.

14. The method according to claim 8, wherein processing the coded values in the signal processing device further comprises:

receiving the coded values at the signal processing device;

multiplying the coded values by coefficients forming a plurality of products;

summing the products to produce a processed signal;

delaying output of the processed signal by a at least one unit delay; and

outputting the processed signal.

15. The method according to claim 14, wherein multiplying the coded values by coefficients forming a plurality of products further comprises:

directing the coded values to a plurality of multipliers and a plurality of sign inverters;

multiplying the coded values by first coefficients in the multipliers to form at least one first product; and

multiplying the coded values by at least one second coefficient in the sign inverters to form at least one second product.

16. A signal processing device comprising:

an input adapted to receive a signal sample;

an encoder adapted to encode the signal sample using a coding process to produce symbolic values;

a processor adapted to modify the symbolic values at least to reduce a number of digits used to represent the symbolic values, produce coded values, and process the coded values in the signal processing device.

17. The device according to claim 16, further comprising:

a plurality of multipliers; and

a plurality of adders, wherein the coded values may be applied as input values to the signal processing device, multiplied by a plurality of coefficients in the plurality of multipliers to create a plurality of products, wherein the products are combined and the processed signal sample undergoes at least one unit delay before being output from the signal processing device.

18. The device according to claim 16, wherein the encoder is adapted to perform a radix 4 Booth coding process.

19. The device according to claim 16, wherein in modifying the symbolic values, the processor is adapted to change at least one value of a digit in the coding process based upon a value in a next higher order digit of the symbolic values to create the coded values.

20. The device according to claim 16, wherein the signal processing device comprises a digital filter.

21. The device according to claim 20, where the digital filter comprises a finite impulse response filter.

22. The device according to claim 16, wherein the signal processing device is also adapted to input the coded values, multiply the coded values by coefficients forming a plurality of products, sum the products to produce a processed signal, delay output of the processed signal by at least one unit delay and output the processed signal.

23. The device according to claim 22, wherein the signal processing device is also adapted to multiply the coded values by first coefficients in the multipliers to form at least one first product; and multiply the coded values by at least one second coefficient in a sign inverters to form at least one second product.